



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/470,542	12/22/1999	DAVID W. FRAME	042390.P7651	6279

7590 12/17/2001

KENNETH M SEDDON
BLAKELY SOKOLOFF TAYLOR & ZAFMAN LLP
12400 WILSHIRE BOULEVARD 7TH FLOOR
LOS ANGELES, CA 90025

EXAMINER

THAI, XUAN MARIAN

ART UNIT	PAPER NUMBER
----------	--------------

2181

DATE MAILED: 12/17/2001

4

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/470,542

Applicant(s)

FRAME ET AL.

Examiner

XUAN M. THAI

Art Unit

2181

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 22 December 1999.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-22 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 16-18 is/are allowed.
- 6) ☒ Claim(s) 1-10, 15, 19, 21 and 22 is/are rejected.
- 7) ☐ Claim(s) 11-14 and 20 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

1. This is in response to communication filed on December 22, 1999. Claims 1-22 are presented for examination.

Specification

2. The disclosure is objected to because it contains an embedded hyperlink and/or other form of browser-executable code. Applicant is required to delete the embedded hyperlink and/or other form of browser-executable code. See MPEP § 608.01.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

Art Unit: 2181

4. Claims 1, 2, 6, 19 and 21 are rejected under 35 U.S.C. 102(e) as being anticipated by Suh (USPN: 6,078,978).

As per claim 1; Suh discloses the invention as claimed including an apparatus comprising: a first integrated circuit (first chip A; figure 5) comprising a Direct Rambus cell would be within the teachings of Suh as Suh discloses that the field of the invention is in a bus interface circuit in a semiconductor memory device and the memory device is the SDRAM or Rambus DRAM (e.g. see col. 1, lines 5-40); a second integrated circuit (second chip B; figure 5) comprising a Direct RAC would be within the teachings of Suh (same as explanation of Direct RAC in the first chip; see col. 1, lines 1-40); a dual-terminated transmission line (bus 12, figure 5; e.g. see col. 5, lines 55 et seq. bridging col. 6, lines 1-19), wherein the dual-terminated transmission line communicatively couples the Direct RAC of the first IC with the Direct RAC of the second IC (e.g. see col. 5, lines 55 et seq. bridging col. 6, lines 1-19).

As per claim 2, Suh discloses wherein the dual-terminated transmission line (12; figure 5) includes a first resistor R_t adjacent to the first IC and a second resistor R_t adjacent to the second IC.

As per claim 6, wherein the second IC comprises a memory repeater hub would be within the teachings of Suh. For example, Suh discloses that chip B (the second IC) comprises of both receivers for receiving data and drivers (drvB1 ... drvBn; repeater ability) for driving data onto bus 12 (see figure 5).

As per claim 19, it encompasses the same scope of invention as to that of claim 1; the claim is therefore rejected for the same reasons as being set forth above with respect to claim 1.

Art Unit: 2181

As per claim 21, Suh discloses the claimed invention including a method of communicating between a first integrated circuit (IC) and a second IC, comprising: providing a dual-terminated transmission line (12; figure 5) communicatively coupling the first IC and the second IC; and transmitting data signals across the dual-terminated transmission line at a rate in excess of 1 Gbytes/sec; for example Suh discloses data transmission rate of 1.6 Gbytes/sec (see col. 1, lines 38-39).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

7. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Suh (USPN 6,078,978) in view of Leung et al. (USPN 6,272,577).

Art Unit: 2181

As per claim 7, Suh discloses the claimed invention as applied to claim 1. However, Suh does not explicitly states the use of source-synchronous communication between the first and the second ICs.

Leung et al. (hereinafter Leung), in his teachings of a data processing system comprising of plurality of memory modules coupled to a master I/O module through a bus, teaches that it is known to utilize a source-synchronous transfer method to communicate between the two modules or integrated circuits (see col. 5, lines 37-40 and col. 19, lines 53-62).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize the teaching of source-synchronous transfer method between two integrated circuits through an interconnecting bus as being taught by Leung in that of the Suh system in order to have the source-synchronous communication between the first and the second integrated circuits. By doing so, it would allow the system of Suh to meet the synchronous and asynchronous operation requirements and can also use the same set of connection pins which would results in smaller IC packaging requirements thus leading to cost and space savings. This method would also be advantageous in that it would results in memory devices that have short access latency and high data bandwidth, thus improving system performance. (See col. 5, lines 37-40 and col. 19, lines 53-62).

7. Claims 8 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suh (USPN 6,078,978) in view of Manning (USPN 6,230,245).

Art Unit: 2181

As per claims 8 and 9, Suh discloses the claimed invention as applied to claim 1.

However, Suh does not explicitly states the use of specific clock speeds in excess of 250 MHZ or in the range of 300 MHZ to 800 MHZ.

Manning, in his teachings of controlling the operations of memories such as DRAM, teaches that it is known to provide a clock signal in excess of 250 MHZ or in the range of 300 MHZ to 800 MHZ (e.g. see figure 3; see cols. 7-8).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize the teaching of providing clock signal excess of 250 MHZ or in the range of 300 MHZ to 800 MHZ in data transfer between different integrated circuitry of memory devices as being taught by Manning in that of the Suh system. By doing so, it would allow the system of Suh to achieve high data transfer speed in a wide bandwidth data transfer system, thus being advantageous.

8. Claims 3-5, 10-15 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suh (USPN 6,078,978) in view of Burns (USPN 6,310,392).

As per claims 3 and 22, Suh discloses the claimed invention as applied to claims 1 and 21, respectively. However, Suh does not explicitly states the value of the resistance of the terminating resistors to be about 25 ohms to 65 ohms or transmission lines with impedances ranging from 45 to 55 ohms.

On the other hand, Burns, in his teaching of Rambus technology, explicitly states that high-speed signals of the Rambus Channel required matched transmission lines with identical propagation characteristics with signals requires matched impedances from 25 ohms to 65 ohms.

Art Unit: 2181

Accordingly, it would have been obvious to one of the ordinary skill in the art at the time the invention was made to utilize the teachings of Burns in the system of Suh, since Burns states that it is a requirement of the Rambus Channel to match the transmission lines impedances in order for the high-speed signals to work properly; that is to reduce reflections of propagating signal transitions which resulted in ringing which causes cross talk which would compromise the integrity of the system (see cols. 1-2). Thus by providing proper termination of the transmission lines, good impedance matching, it would eliminate such undesired crosstalk and improve system performance and integrity. Therefore being advantageous.

As per claims 4 and 5; the transmission line impedance and the resistance values of the first resistor would be within the teachings of Suh and Burns see Burns col. 8, lines 32-35 and col. 11, lines 25-29.

As per claims 10 and 15, states a mezzanine card having a connector and comprising the second integrated circuit, wherein the connector is adapted to be communicatively coupled to a third integrated circuit and the third circuit comprises a Rambus module communicatively coupled to the connector.

Burns, in his teachings of stacked micro ball grid array packages, states several embodiments as examples e.g.

"One embodiment of the present invention has chip scale packages mounted to the upper surface of a flexible substrate. Package lead pads formed in the flexible substrate electrically couple to select package leads. A portion of each flexible substrate extends away from the integrated packages and includes circuit interconnect pads (e.g. connector) located on the lower surface for electrical and thermal coupling to corresponding interconnect pads on the support substrate. Another embodiment of a flexible substrate of the present invention, has the extended portion folded back, at a 180 degree, angle to itself, allowing circuit interconnect pads on the upper surface of the flexible substrate to couple with corresponding interconnect pads on the support substrate. An alternative embodiment provides two chip scale packages mounted to opposite sides of two adjacent flexible substrates, each of which is coupled to a different one of the

Art Unit: 2181

package's leads. The extended portion of each flexible substrate attaches to the support substrate." (Col. 2, lines 48-65). Also see for examples figures 3 and 4.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to employ the teachings of a mezzanine card with a connector and Rambus module coupled to the connector as taught by Burns in the system of Suh, since Burns states that such methods would "enable economical manufacture of multi-package modules comprised of chip-scale packages and provide enhanced thermal characteristics, while maintaining high quality transmission lines required for RAMBUS CHANNEL." (see col. 2, lines 28-33).

Allowable Subject Matter

8. Claims 16-18 are allowed.
9. Claims 11-14 and 20 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The references are cited in the Form PTO-892 for the applicant's review.

Art Unit: 2181

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Xuan M. Thai whose telephone number is (703) 308-2064. The examiner can normally be reached on Tuesday-Friday and on alternate Monday from 8:30 a.m. to 6:00 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner supervisor, Robert W. Beausoliel, can be reached on (703) 305-9713.

The fax phone numbers for the organization where this application or proceeding is assigned are as follows:

(703) 746-7238	[After Final Communication]
(703) 746-7239	[Official Communication]
(703) 746-7240	[For Status inquiries and draft communication]

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-3900.



XUAN M. THAI
Primary Examiner
Art Unit 2181

XMT
December 12, 2001